

Remote Wake-Up

Intel Corporation

September 29, 1997



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Agenda

- **RWU purpose and popular topics**
- **RWU and standard LOM/NIC**
- **RWU design considerations**
- **Networking support model**

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RWU Purpose and Popular Topics



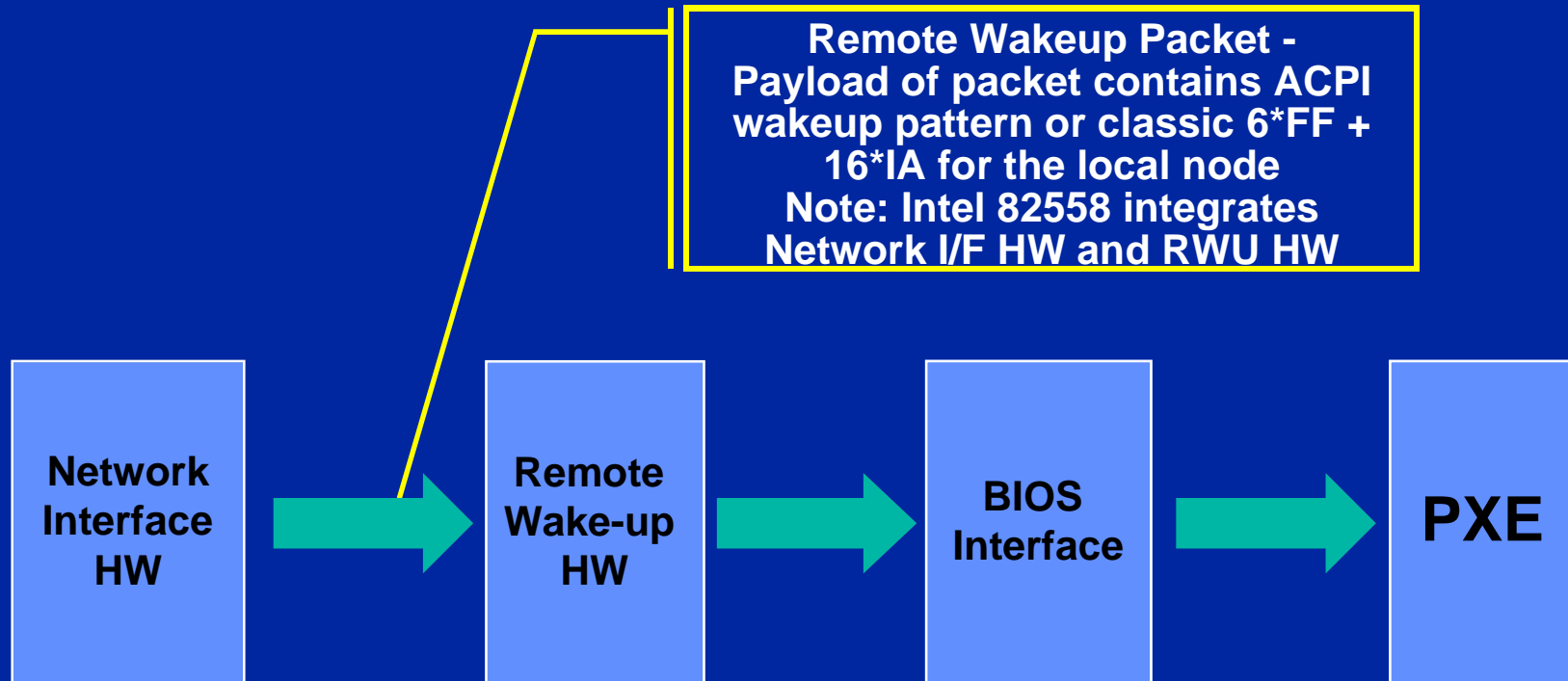
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RWU and Manageability

- **RWU and PXE provide the first two fundamental building blocks of WFM**
 - ◆ **Remote boot and remote network connection**
- **RWU provides the first link to WFM**
 - ◆ **The ability to power-down a system and still remain virtually connected to manageability services**
- **RWU is a requirement for NetPCs**
- **RWU is OS-independent and can be functional without ever previously booting the PC**
- **For OS upgrades/installs, RWU is the key to “out of the box” WFM-ready systems**



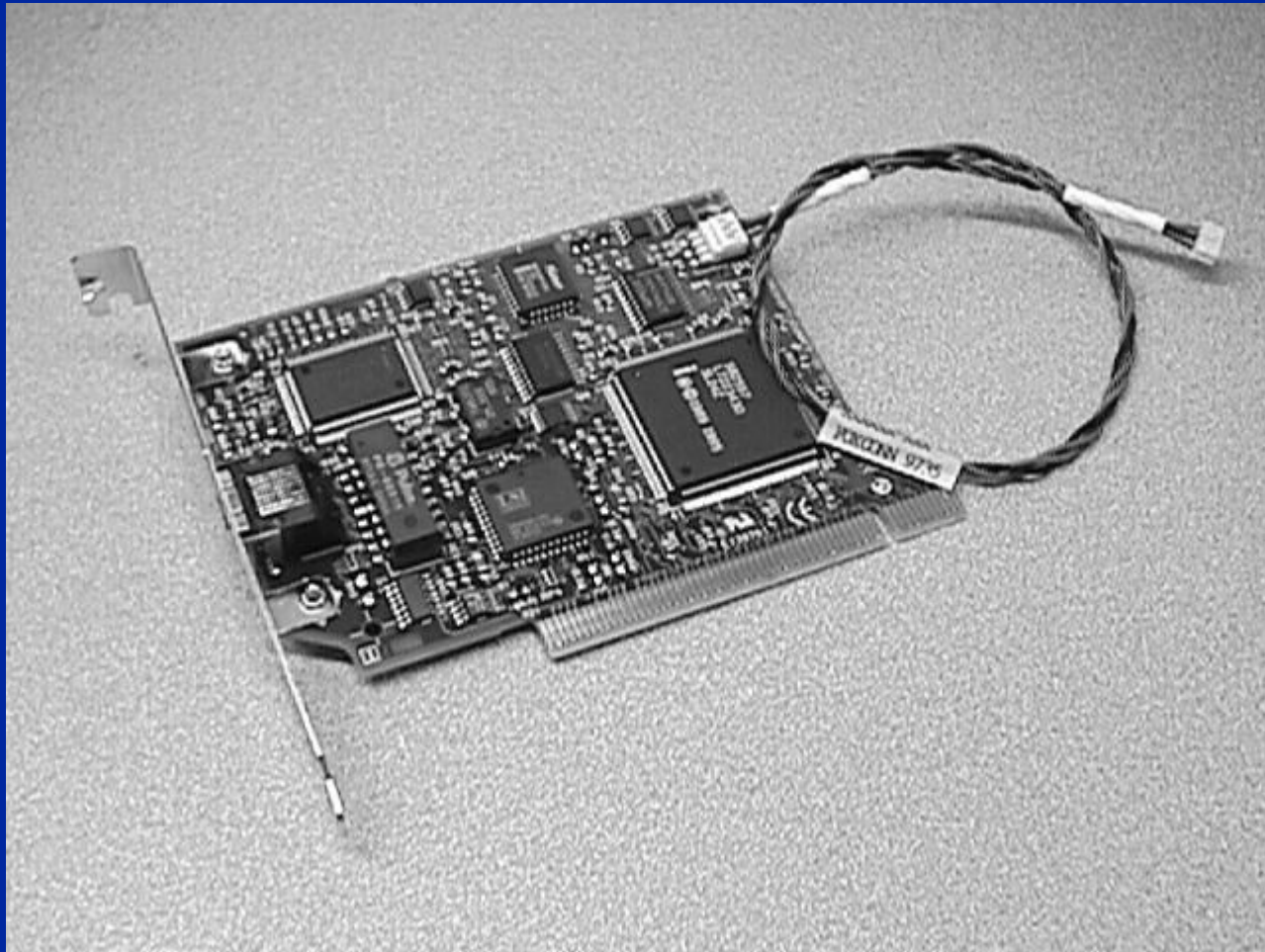
Remote Wake-up



RWU Flavors

- **RWU can be implemented as a NIC (Network Interface Card) or LOM (LAN-On-Motherboard)**
- **The RWU NIC requires certain system modifications - no easy install**
- **The RWU LOM also requires modifications, but these are incorporated during the design cycle**

WOL Header



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Then Why LOM?

- LOM reflects the trend in sharing network manageability between networking silicon and the chipset
- Avoids non-standard cabling used for RWU NICs
- Compatibility within system is assured
- Allows further integration with system capabilities
- Allows network performance tuning

RWU in the APM Context

- **APM represents existing (legacy) power management implementations - linked to, say, Windows* 95 Suspend mode functionality**
- **APM is implemented at BIOS level**
- **APM performs power management at a system level (no device level granularity in power control)**
- **APM typically supports:**
 - ◆ **Full power**
 - ◆ **Screen saver mode**
 - ◆ **Suspend mode**
 - ◆ **No power states**
- **APM triggers wake from suspend for events like keyboard or mouse activity - configurable**
- **RWU wakes the system from the no power or suspend modes - depending on configuration**
- **Intel 82557 and 82558 support APM RWU and can HW-initialize**



RWU in the ACPI Context

- **ACPI represents future power management implementations - linked to 1998 MS OSs**
- **ACPI is implemented at OS level**
- **ACPI performs power management at a system, bus, or device level**
- **ACPI supports:**
 - ◆ **System power management (G0-3/S0-3)**
 - ◆ **Bus power management (B0-3)**
 - ◆ **Device power management (D0-3)**
- **ACPI triggers a change in power management state based on well-defined OS policies**
- **In an ACPI OS, RWU functions as one of multiple wake events capable of changing the system/bus/device power management state**
- **Intel 82558 is fully ACPI-compliant, supports D0-3 device states, wake events in all states, and provides a low cost/power single chip networking solution for WFM**



RWU LOM/NIC and Standard LOM/NIC

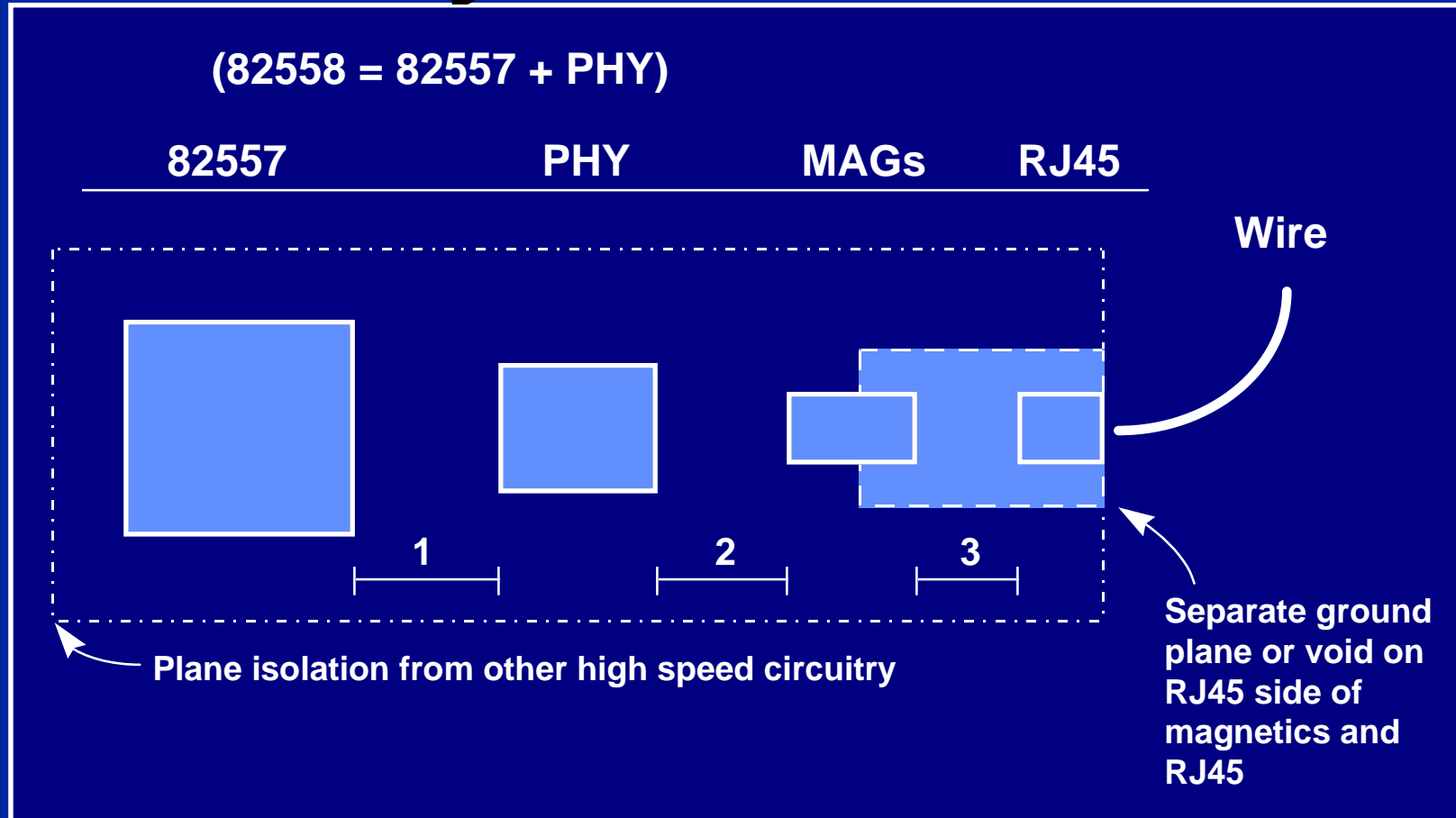
- RWU uses all of the same support and implementation tools as a standard LOM
- RWU takes advantage of the drivers, compatibility history, and support of NIC SW
- A networking solution providing RWU should behave exactly the same during normal traffic as a networking solution with the same component and without RWU
- RWU solutions require different power solutions, additional receiver circuits, and special attention to the existence of powered-up and powered-down circuits in close proximity

RWU Design Considerations



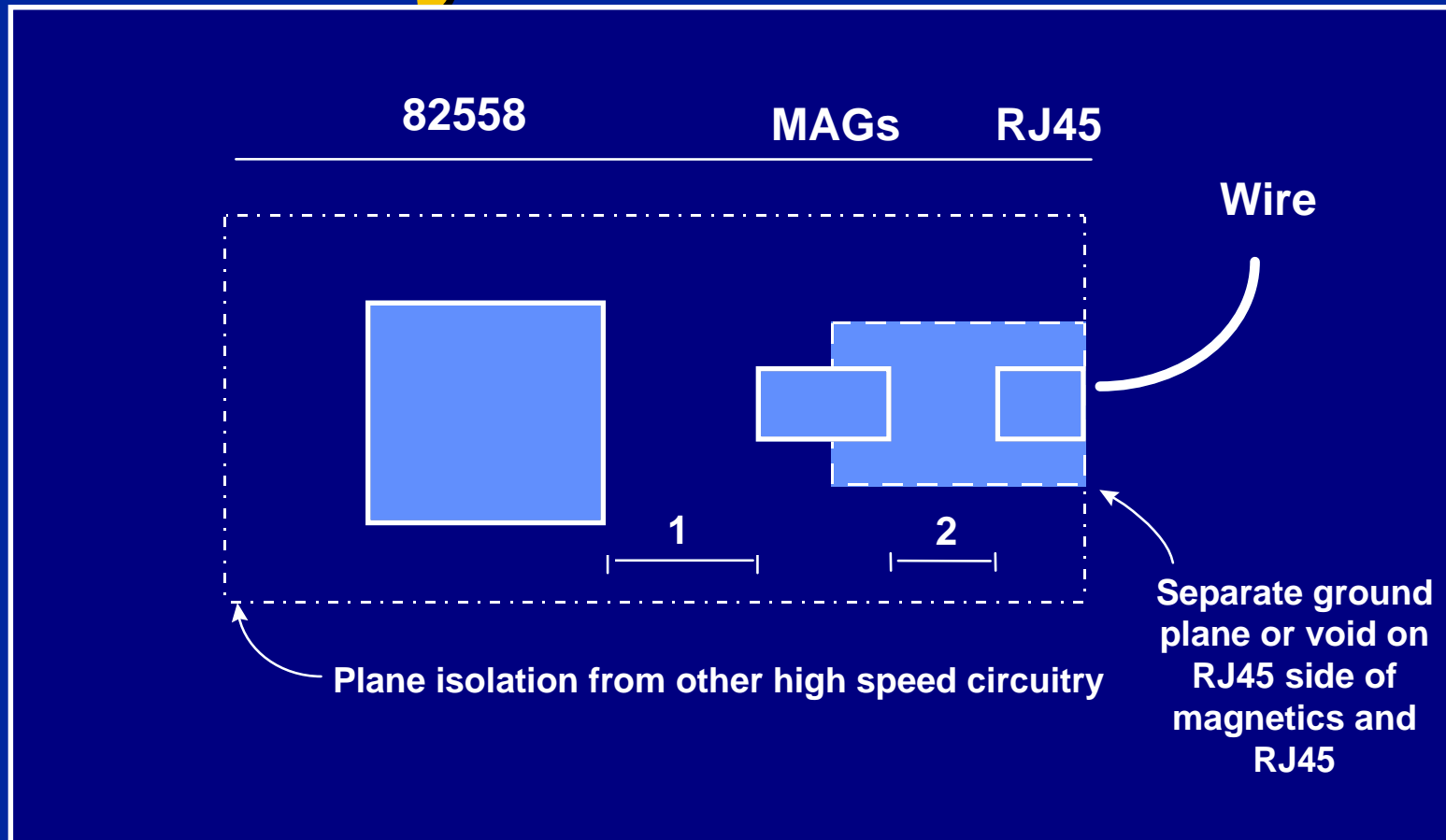
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82557 Layout Considerations



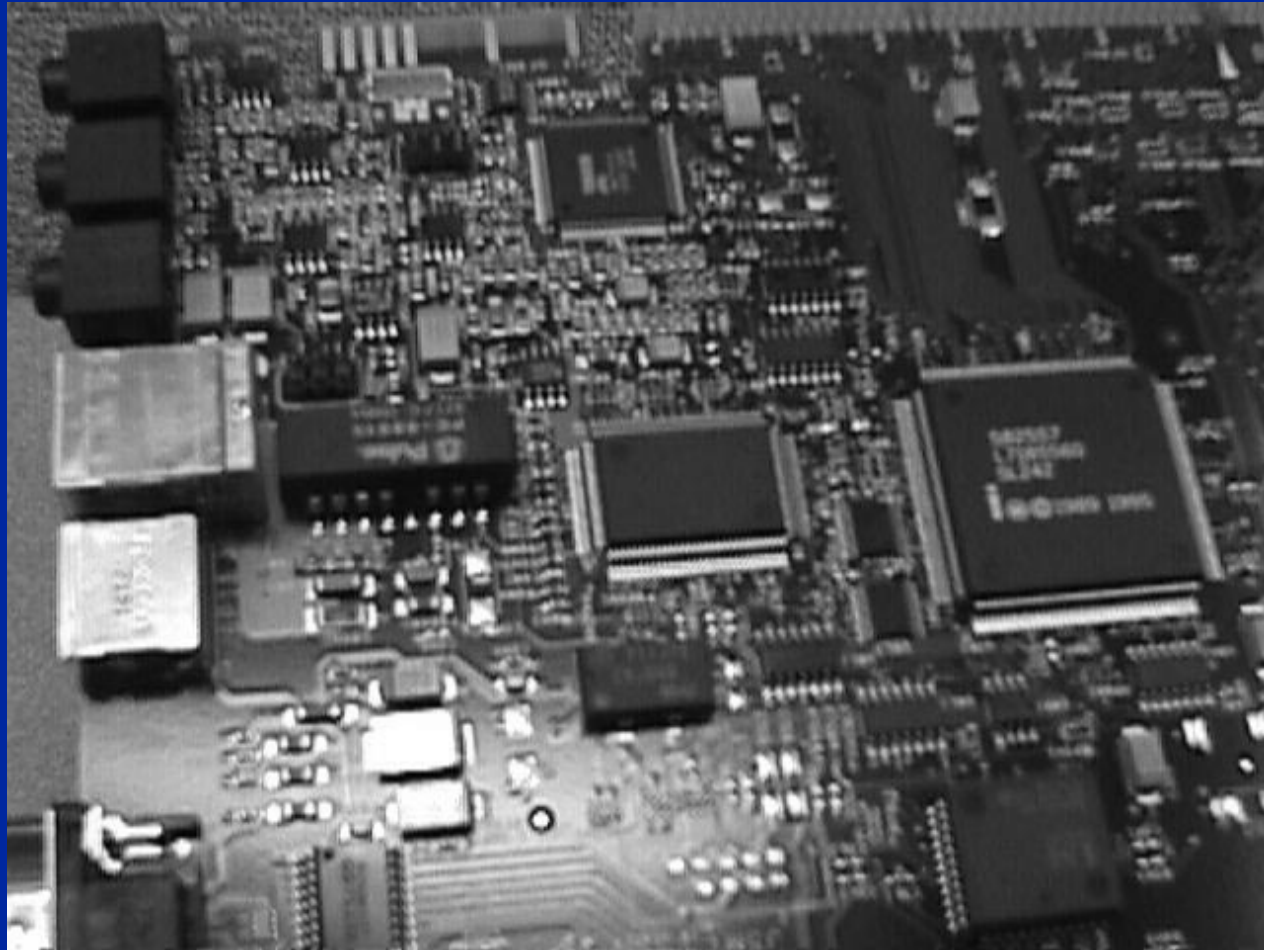
- 1 - MII signals; minimize length; 68 Ohm traces; priority 3.
- 2 - PHY->Mag signals; <1" length; route pairs together; 50 Ohm traces; priority 2.
- 3 - Mag ->RJ45 signals; shortest length possible; route pairs together; 50 Ohm traces; Priority 1. If these traces must be longer, identical trace geometries must be observed to avoid reflections and return loss failures.

82558 Layout Considerations



- 1 - 82558->Mag signals; <1" length; route pairs together; 50 Ohm traces; Priority 2.
- 2 - Mag ->RJ45 signals; shortest length possible; route pairs together; 50 Ohm traces; Priority 1. If these traces must be longer, identical trace geometries must be observed to avoid reflections and return loss failures.

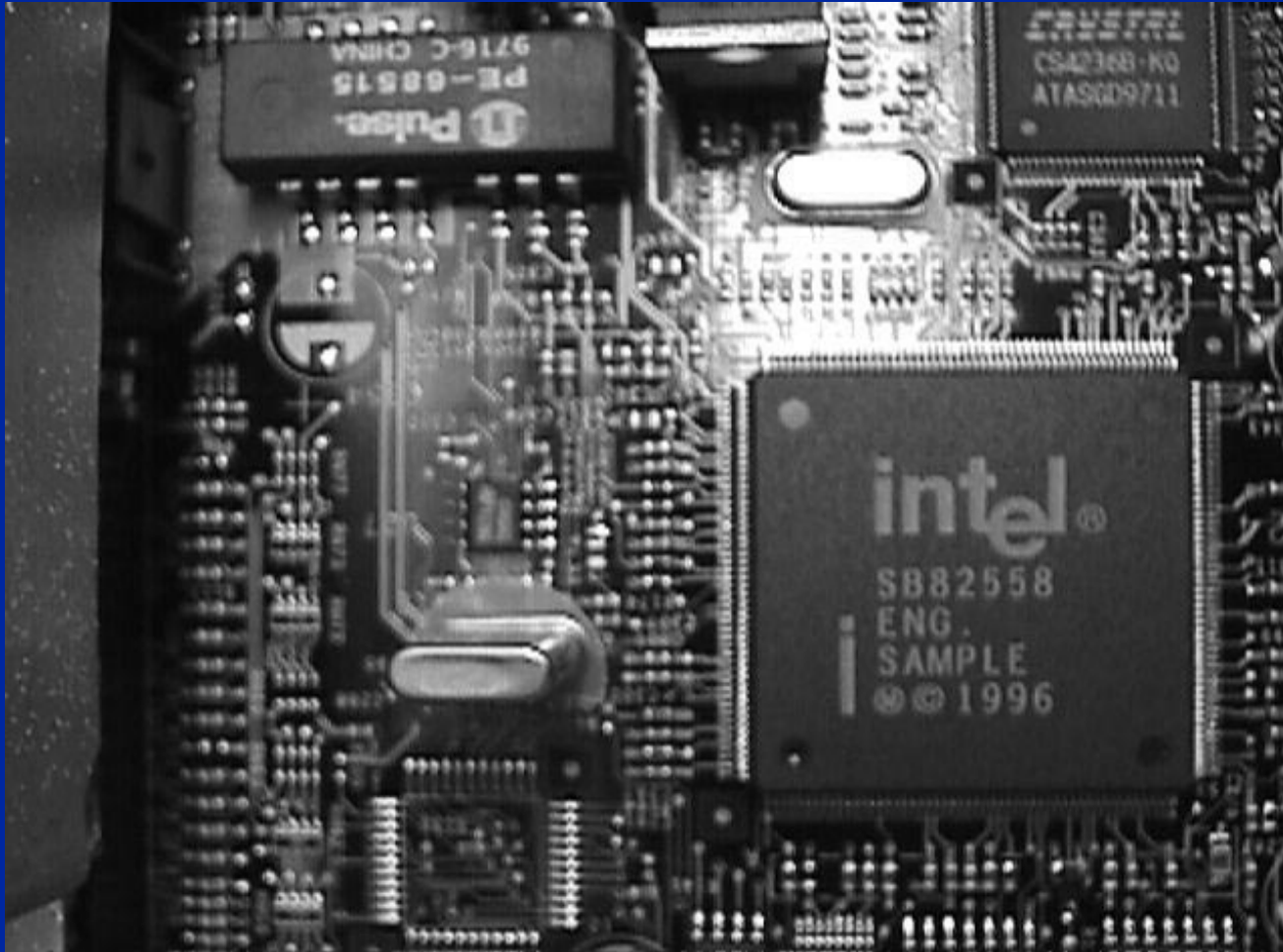
82557 And 82558 Implementation



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82558 Implementation



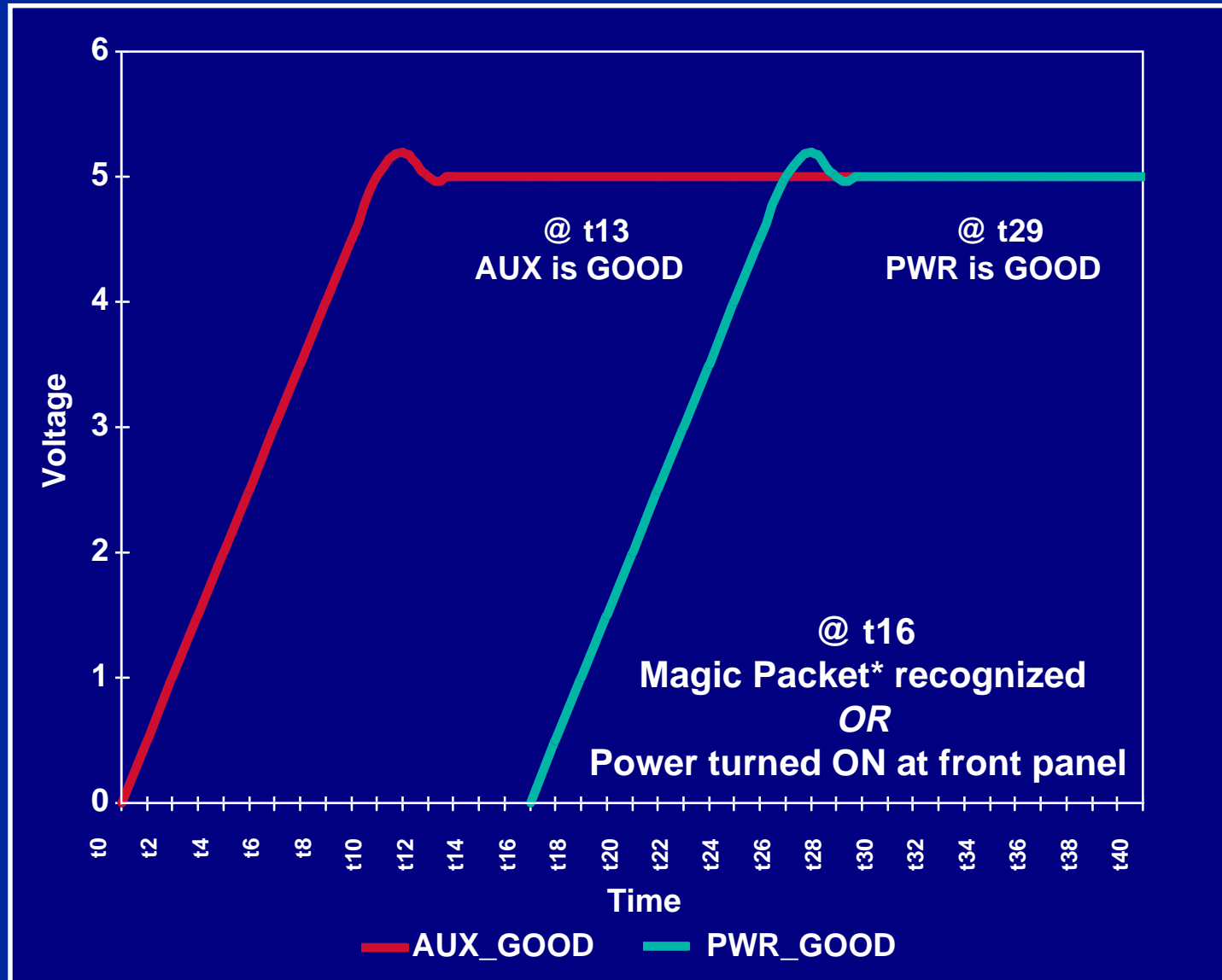
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Power Supplies and Connectors

- All power supplies supply some amount of auxiliary current for support circuitry (usually under 50mA)
- RWU designs require an increase in this auxiliary supply to an optimal level of 720mA
- RWU designs are simplified if there is a supply valid signal provided for Main and Aux power
- There are a number of existing connectors for RWU
 - ◆ Different RWU solution providers use different connectors
 - ◆ Intel helped define single 3 pin connector as an industry standard (see spec in CD)

Power Supply Characteristics



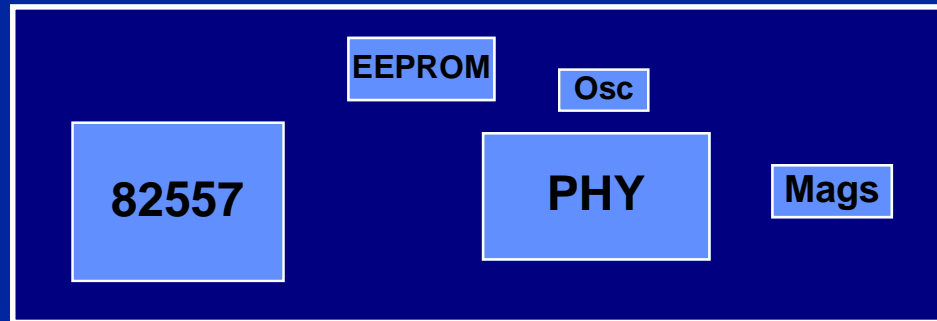
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RWU Planes and State Indicators

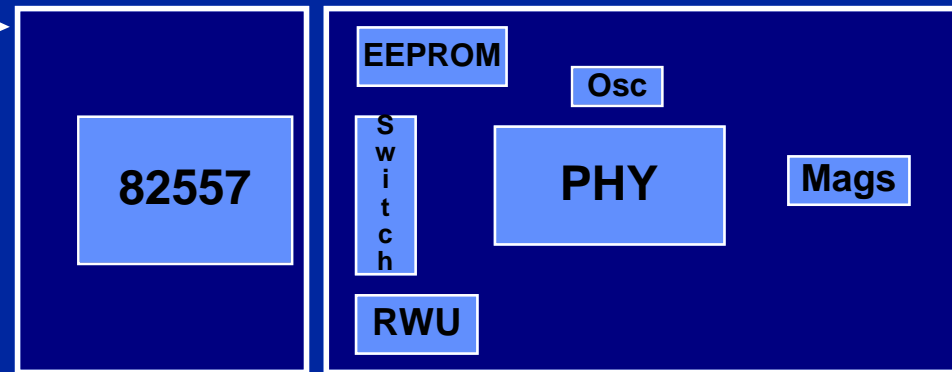
- Aux and Main power planes
- Auxgood and PWRgood indicator circuits
- 82557 isolation circuitry and its integration into the 82558
- Avoid Plane bleed-thru and component damage
- FET switching between planes to support all modes

LOM and RWU Power Planning

LOM



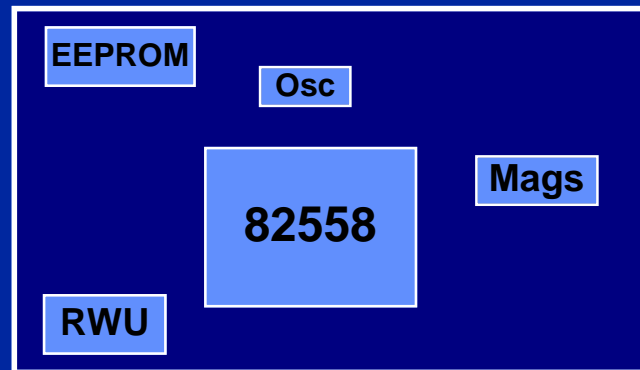
5V or main supply RWU



5V or main supply

Aux5 or secondary supply

RWU

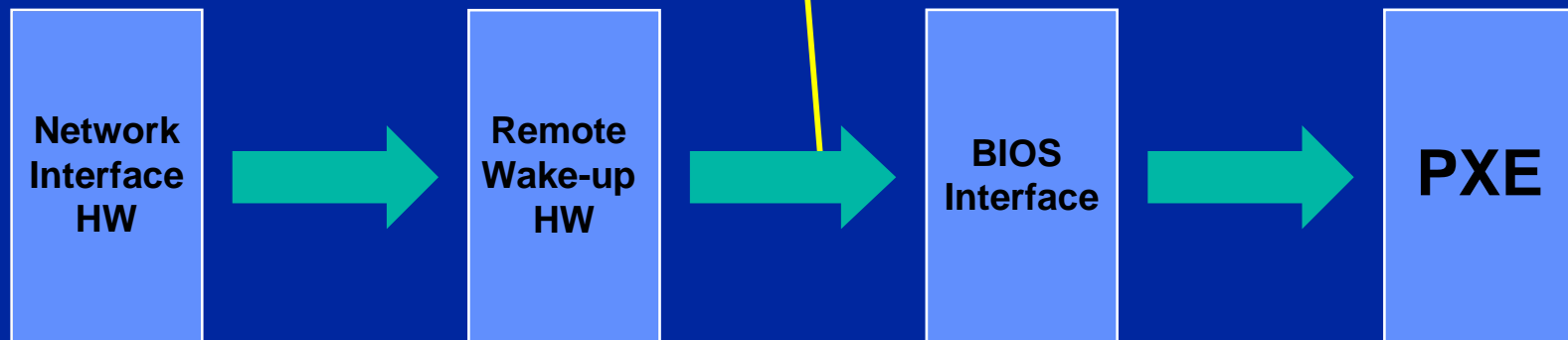


Aux5 or secondary supply



Remote Wake-up

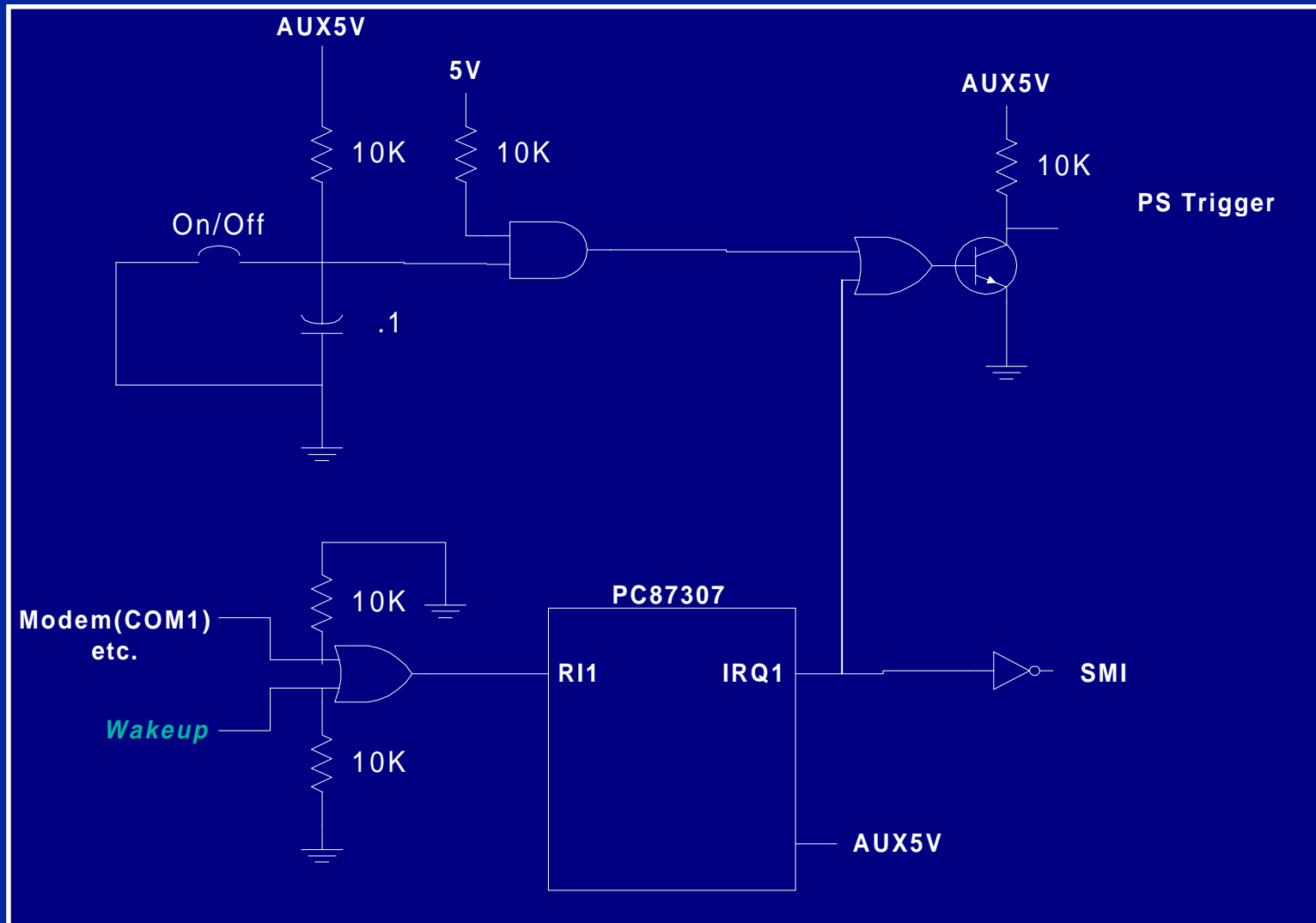
Wakeup signal generated to SuperIO,
PIIX4, or discrete power solution.
Depending on implementation, status is
stored to be retrieved by BIOS during boot



Wakeup Signal Receiver Circuits

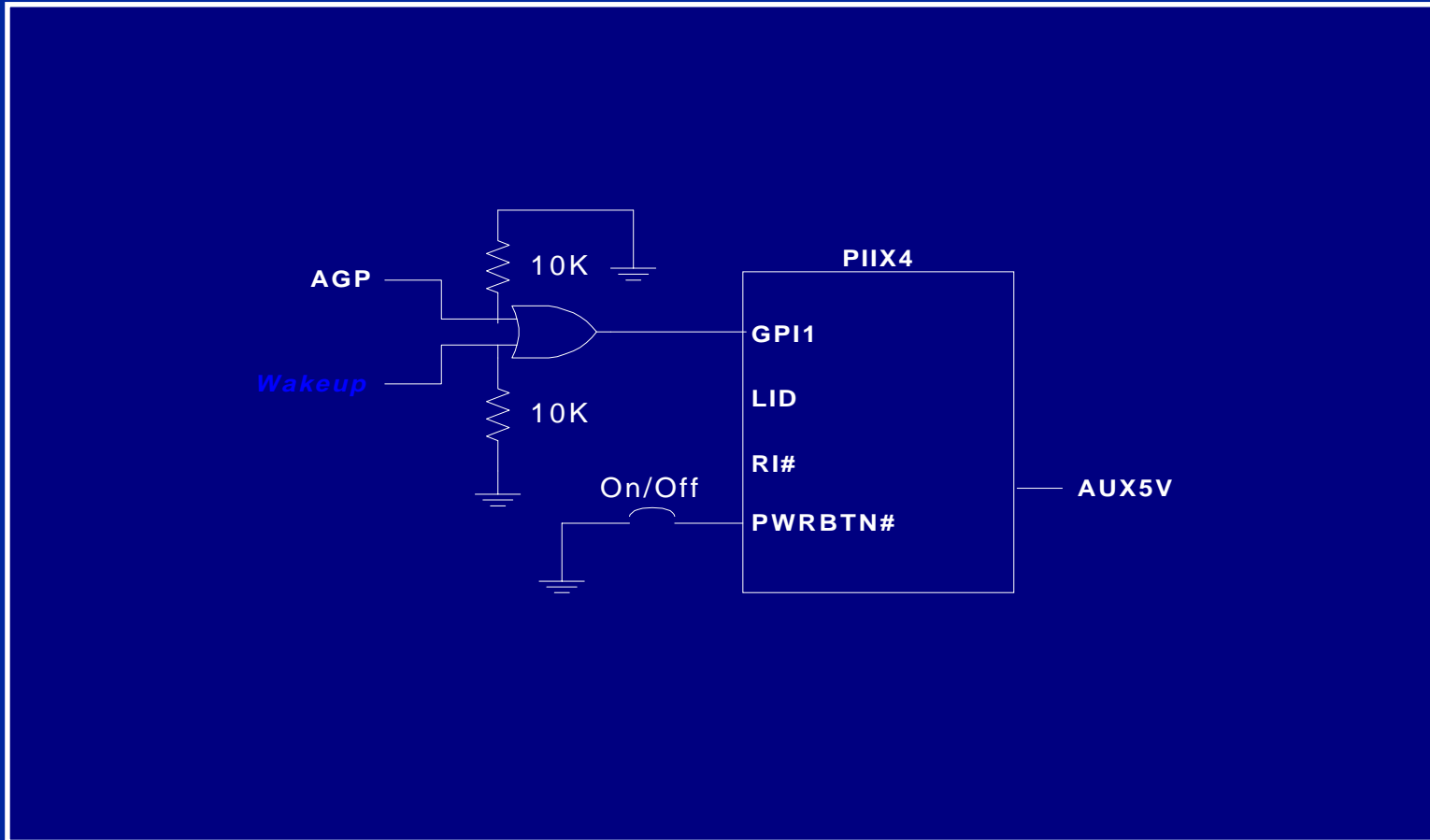
- **Implementations:**
 - ◆ **Power supply switch**
 - ◆ Not forward compatible
 - ◆ Not configurable to disable or get status
 - ◆ **SuperIO ring indicator**
 - ◆ Exists in current designs already
 - ◆ Configurable and Status friendly
 - ◆ **PIIX4 ring indicator**
 - ◆ Exists in current designs already
 - ◆ Configurable and Status friendly

SuperIO



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PIIX4



RWU Testing and Validation

- False packets (15 IAs, 5 “FF”s, etc.)
- Marginal voltage level testing
- High network traffic behavior
 - ◆ RWU
 - ◆ Normal LAN
- Power cycling behavior
- IPSL segment will give greater detail

BIOS Hooks

- Stores the occurrence of a wake event for post-boot use
- Allows control of what functionality provides RWU functionality (LAN, modem, etc.)
- BIOS section will cover in more detail

Determine Source of Current Wake-Up

Enter:

AX := 2307h

BX := 5755h

Int 15h

Exit:

CY := 0 (Success)

AH := 00h (Success)

CL (bits 2-0) := 6 (Power Switch)

CL (bits 2-0) := 5 (LAN)

CL (bits 2-0) := 4 (COM1 RING)

CL (bits 2-0) := 3 (Timer)

CY := 1 (Failure)

AH := 86h (Unsupported function)

All other registers are unchanged.

Set Source of Next Wake-Up

Enter:

AX := 2308h

BX := 5755h

Int 15h

Exit:

CY := 0 (Success)

AH := 00h (Success)

CL (bits 7-3) := Unchanged from Determine Source of Wake-up

CL (bits 2-0) := New wake-up source (see above)

CY := 1 (Failure)

AH := 86h (Unsupported function)

All other registers are unchanged.



Networking Support Model

- **Don't be an alpha site for first LOM designs -**
 - ◆ Intel is currently supporting their third generation of successful 10/100 designs (with the 82558)
- **Make sure they have top of the line SW -**
 - ◆ Intel is the market segment share leader in 10/100 solutions
- **Make sure they can meet demand**

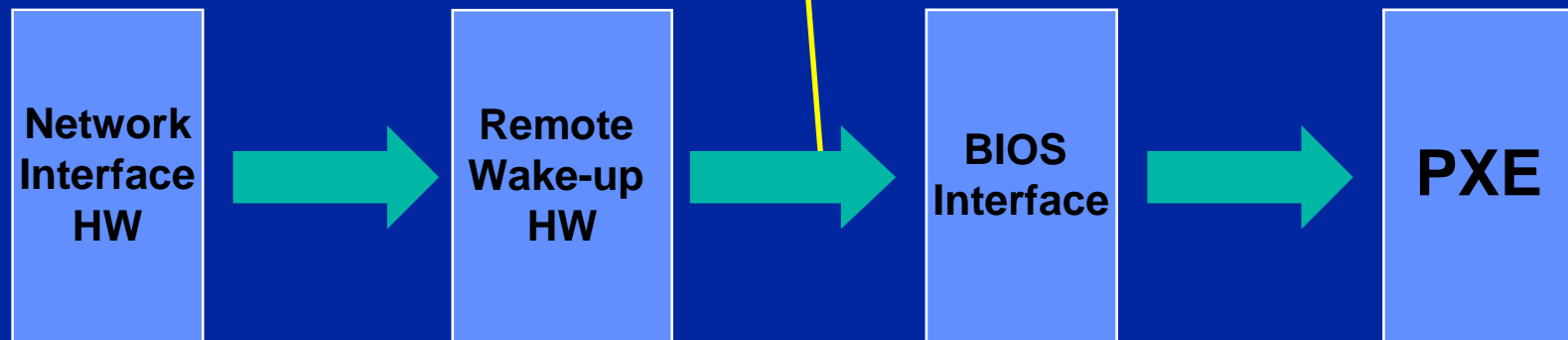


Networking Support Model

- **Make sure they provide competitive and timely solutions -**
 - ◆ **Intel provides high performance/low cost workgroup components (hubs, switches, downlinks, etc.)**
 - ◆ **Intel is developing and providing next - generation network manageability solutions**

Remote Wake-up

Wakeup signal generated to SuperIO, PIIX4, or discrete power solution. Depending on implementation, status is stored to be retrieved by BIOS during boot



Summary

- **RWU is a fundamental building block of WFM.**
- **LOM is simpler path to RWU**
- **RWU is easy if guidelines followed**
- **Choose networking vendor carefully**

Collateral

- **Wired for Management Baseline**
- **Wake-On-LAN (WOL) Header Recommendations**
- **Intel 82557 Fast Ethernet PCI Bus LAN Controller Data Sheet**
- **Wake On LAN Design Guidelines**
- **Intel 82558 Fast Ethernet LAN Controller with Integrated PHY**



Backup



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LOM/WOL Milestones

- Collateral provided
- First schematics/layout provided
- First schematics/layout reviewed
- First units provided
- First units IEEE and functional test
- Design adjustments made
- FCS units provided
- FCS unit IEEE and functional test
- Certification

When Certification is Needed

- **HW and EMI/Environment**
 - ◆ When the PBA rolls (the schematic has changed and a new layout generated)
- **SW**
 - ◆ When the executable size and date change (run-time code changes have occurred)

Engineering Support

- **Multiple Support Channels**
 - ◆ **1-800 Intel Applications Support**
 - ◆ **Factory TME Support**
 - ◆ **Factory Application (NIC) Design Engineering Support**
 - ◆ **Chip Design Engineering Support**



Network Functional Tests

- Flash presence
- Test and program EEPROM with ENET
- Init and configure MAC
- Test Interrupts
- 10 and 100 MBit line speed configure
- Autonegotiation test
- 10 and 100 MBit internal loopback test
- 10 and 100 MBit PHY loopback test
- 10 and 100 MBit board to board function test
- Confirm EEPROM ENET value

General PHY Characteristics

	Avail	Speed	FDX	Driver Support	Power	# chips	Interface
82558	Now	10/100	Yes	Yes	230mA	1	MII
82555	Now	10/100	Yes	Yes	275mA	1	MII
ICS1890	Now	10/100	Yes	Yes	360mA	1	MII
83840	Now	10/100	Yes	Yes	560mA	2	MII



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Generic BOMs for PHY implications

82558 BOM

20 resistors
7 capacitors
1 crystal
3 LEDs
Mags

82555 BOM

14 resistors
9 capacitors
1 crystal
2 inductors
3 LEDs
Mags

1890 BOM

21 resistors
5 capacitors
1 crystal
3 inverters
3 LEDs
Mags

83840 BOM

42 resistors
8 capacitors
2 crystals
4 transistors
3 LEDs
Filter